WHAT WE CLAIM ARE:

1. A semiconductor device manufacture method comprising steps of:

(a) forming a gate electrode over each of a plurality of active regions defined in a silicon substrate, said gate electrode traversing a corresponding one of the active regions, and forming extension regions of source/drain in the active region on both sides of said gate electrode;

(b) depositing first and second insulating films having different etching characteristics on the silicon substrate, said first and second insulating films covering side walls of said gate electrode, and anisotropically etching said first and second insulating films to form a side wall spacer on the side walls of each gate electrode;

(c) selectively etching said first insulating film of the side wall spacer to form a retraction portion retracted from a surface of said second insulating film on a gate electrode side and on a silicon substrate side;

(d) implanting ions into the silicon substrate by using the side wall spacer as a mask to form source/drain regions in the silicon substrate; and

(e) depositing metal capable of silicidation over the silicon substrate and performing a silicidation reaction and form silicide regions.

2. The semiconductor device manufacture method according to claim 1, wherein selective etching at said step (c) is isotropical etching.

3. The semiconductor device manufacture method according to claim 2, wherein said first insulating film is made of silicon oxide, said second insulating film is made of silicon nitride, and said step (c) selectively wet-etches silicon

oxide with dilute hydrofluoric acid aqueous solution.

4. The semiconductor device manufacture method according to claim 1, wherein said step (c) side-etches said first insulating film at least by 10 nm and at most 0.6 times a width of the side wall spacer.

5. The semiconductor device manufacture method according to claim 1, wherein the plurality of active regions include n- and p-channel regions, said step (d) includes a step of obliquely implanting n-type impurity ions into the n-channel region, while p-type impurity ions are implanted into the p-channel region only at an angle nearer to a substrate normal than the oblique ion implantation.

6. The semiconductor device manufacture method according to claim 5, wherein said step (d) includes a step of obliquely implanting n-type impurity ions into the n-channel region and a step of vertically implanting n-type impurity ions into the n-channel region.

7. A semiconductor device manufacture method according to claim 1, wherein said step (e) sputters Co or Ni on the silicon substrate and also in the retraction portion on the silicon substrate side, and forms the silicide region also on the silicon substrate under the retraction portion and a thicker silicide region on the silicon substrate outside of the side wall spacer.

8. The semiconductor device manufacture method according to claim 1, further comprising a step of:

(f) after said step(e), depositing a third insulating film on the silicon substrate, the third insulating film entering the retraction portion and burying the retraction portion.

9. A semiconductor device manufacture method comprising steps of:

(a) forming a gate electrode in each of a plurality of active regions defined in a silicon substrate, said gate electrode traversing the active region, and forming extension regions of source/drain in the active region on both sides of said gate electrode;

(b) depositing first and second insulating films having different etching characteristics on the silicon substrate, said first and second insulating films covering side walls of said gate electrode, and anisotropically etching said first and second insulating films to form a side wall spacer on the side walls of each gate electrode;

(c) selectively etching said first insulating film of the side wall spacer to form a retraction portion retracted from a surface of said second insulating film on a side surface and an upper surface of the side wall spacer;

(d) implanting ions into the silicon substrate by using the side wall spacer as a mask to form source/drain regions in the silicon substrate; and

(f) depositing a third insulating film on the silicon substrate, the third insulating film entering the retraction portion and burying the retraction portion.

10. The semiconductor device manufacture method according to claim 9, wherein the plurality of active regions include n- and p-channel regions, said step (d) includes a step of obliquely implanting n-type impurity ions into the n-channel

region, and implanting p-type impurity ions into the p-channel region only at an angle nearer to a substrate normal than the oblique ion implantation.

11. The semiconductor device manufacture method according to claim 10, wherein said step (d) includes a step of obliquely implanting n-type impurity ions into the n-channel region and a step of vertically implanting n-type impurity ions into the n-channel region.

12. The semiconductor device manufacture method according to claim 9, further comprising a step of:

(e) after said step (d), depositing metal capable of silicidation over the silicon substrate by sputtering, and performing a silicidation reaction and form silicide regions.

13. The semiconductor device manufacture method according to claim 12, wherein the metal capable of silicidation is cobalt or nickel.

14. The semiconductor device manufacture method according to claim 10, further comprising a step of:

(e) after said step (d), depositing metal capable of silicidation over the silicon substrate by sputtering, and performing a silicidation reaction and form silicide regions.

15. The semiconductor device manufacture method according to claim 14, wherein the metal capable of silicidation is cobalt or nickel.

16. A semiconductor device comprising:

a silicon substrate having a plurality of active regions;

an insulated gate electrode formed on said silicon substrate and traversing a corresponding one of the active regions;

a side wall spacer formed on side walls of said insulated gate electrode and made of a lamination of first and second insulating films having different etching characteristics, said side wall spacer having retraction portions at the end face of the first insulating film retracted from a surface of the second insulating film; and

a silicide region formed on a surface of said silicon substrate under the retraction portion and a thicker silicide region formed on the surface of said silicon substrate in an outer area of said silicide region.

17. The semiconductor device according to claim 16, wherein said insulated gate electrode includes a polysilicon layer, and polysilicon which contacts the retraction portion in an upper region of the said side wall spacer is silicidated.

18. The semiconductor device according to claim 16, further comprising a third insulating film deposited on said silicon substrate and burying the retraction portion.

19. The semiconductor device according to claim 17, further comprising a third insulating film deposited on said silicon substrate and burying the retraction portion.